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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/664,912	KIM ET AL.	
	Examiner	Art Unit	
	Tammy Pham	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 Feb 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-12,14-32 and 34-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-12,14-32 and 34-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 23 February 2007 has been entered.

Response to Amendment

2. Claims 4, 13, 33 have been cancelled. Claims 1-3, 5-12, 14-32, 34-47 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-2, 5-8, 30-31, 34, are rejected under 35 U.S.C. 103(a) as being unpatentable over Cairns et al. ("Cairns1") (US Patent Application: 2002/0030652 A1) in view of Cairns et al. ("Cairns2") (US Patent No: 6,268,841 B1) and Enami et al (US Patent No: 5,892,493).

As for independent claim 1, Cairns1 teaches of a data driving apparatus (Fig. 1, item 2) for a liquid crystal display device (Fig. 1), comprising: a first multiplexer (Fig. 4, item 13) part

performing a time-division on inputted digital pixel data; a digital-analog converter (Fig. 4, item 12) part converting the time-divided digital pixel data from the first multiplexer (Fig. 4, item 13) part to analog pixel signals; a demultiplexer (Fig. 4, item 14) part supplying the analog pixel signals from the digital-analog converter (Fig. 4, item 12) part to a plurality of output channels in section [0015].

Cairns1 fails to teach of an output part sampling and holding first received analog pixel signals from the demultiplexer part and holding second received analog pixel signals and simultaneously outputting both first and second received pixel signals to corresponding data lines, wherein the output part comprises: a sampling part sampling the pixel signals from odd-numbered or even-numbered output channels of the demultiplexer part; a capacitor part receiving and holding the sampled pixel signals from the output channels of the demultiplexer part; an output buffer part coupled to the capacitor part.

Cairns2 teaches of an output part sampling and holding (Fig. 11b) first received analog pixel signals from the demultiplexer part (Fig. 4, item 32) and holding second received analog pixel signals and simultaneously outputting both first and second received pixel signals to corresponding data lines (Fig. 11b, item 8); wherein the output part (Fig. 11b) comprises: a sampling part (Fig. 11b, item 47) sampling the pixel signals from odd-numbered or even-numbered output channels of the demultiplexer (Fig. 4, item 32) part; a capacitor part (Fig. 11b, items C1, B2) receiving and holding the sampled pixel signals from the output channels of the demultiplexer part (Fig. 4, item 32); an output buffer (Fig. 11b, item 40) part coupled to the capacitor part (Fig. 11b, items C1, B2, column 10, lines 18-41).

It would have been obvious to one with ordinary skill in the art at the time the invention was made to combine the output part of Cairns2 with the rest of the components of the data driving apparatus of Cairns1 in order to have fewer converters (Cairns2, column 4, lines 33-35).

Cairnes1 and Cairnes2 fails to teach of a third multiplexer part simultaneously discharging the pixel signals held in the capacitors to the corresponding data lines through the output buffer part.

Enami teaches of a third multiplexer part (Fig. 1, item 38) simultaneously discharging the pixel signals held in the capacitors (Cairnes2, Fig. 11b, items C1, B2) to the corresponding data lines through the output buffer part (Cairnes2, Fig. 11b, item 40).

It would have been obvious to one with ordinary skill in the art at the time the invention was made to include a third multiplexer as taught by Enami with the data driver of Cairns1 and the output part of Cairns2 in order to allow the apparatus to perform multiplex driving in which the data voltage is sequentially applied to a number of data lines in each of the data groups (Enami, column 3, lines 49-51).

As for independent claim 30, in addition to the rejection of claim 1 above, Cairns1 as modified by Cairns2 further teaches that the sampling and holding (Cairns2, Fig. 11b) first inputted pixel signals through a first part of the output channels and holding second inputted pixel signals from a second part of the output channels during a first horizontal period, and simultaneously supplying the first and second held pixel signals corresponding data lines (Cairns2, Fig. 11b, item 8, column 6, lines 51-56) during a second horizontal period.

As for claim 2, Cairns1 teaches that the digital-analog converter (Fig. 4, item 12) part coupled to the output channels of the demultiplexer (Fig. 4, item 14) part in section [0015].

As for claim 5, Cairns1 teaches of a shift register (Fig. 4, item 10) sequentially shifting an input source start pulse in accordance with an input source shift clock to generate a sampling signal; and a latch part (Fig. 4, item 11) sequentially latching the pixel data in response to the sampling signal and simultaneously providing the latched pixel data to the first multiplexer (Fig. 4, item 13) during an enable period of an input source output enable signal in section [0015].

As for claim 6, Cairns1 as modified by Cairns2 and Enami teaches of the second multiplexer (Cairns2, Fig. 11b, items 47, 49) provides the corresponding data lines with the pixel signals held in the capacitors (Cairns2, Fig. 11b, items 48, 50) for the enable period of the source output enable signal and a reference voltage of liquid crystal cells for the disabled period of the source output enable signal.

As for claim 7, Cairns1 teaches that the first multiplexer (Fig. 4, item 13) and the demultiplexer (Fig. 4, item 14) part are controlled by an ODD/EVEN signal which performs the time-division for a horizontal period in section [0051].

As for claim 8, Cairns1 as modified by Cairns2 and Enami teaches that the sampling switches controlled by an ODD/EVEN signal which performs the time-division on a horizontal period in Cairns2, column 1, lines 54-58.

As for claim 31, Cairns1 as modified by Cairns2 and Enami Cairns2 teaches that the first and second held pixel signals are supplied to the corresponding data lines for an enable period of an input source output enable signal and a reference voltage of liquid crystal cells is commonly supplied to the corresponding data lines for a disable period in Cairns2, Fig 12.

As for claim 34, Cairns1 teaches that the sampling the pixel signals is controlled by an ODD/EVEN signal performing a time-division on a horizontal period in section [0065].

4. Claims 3, 32, are rejected under 35 U.S.C. 103(a) as being unpatentable over Cairns et al. ("Cairns1") (US Patent Application: 2002/0030652 A1), in view of Cairnes et al. ("Cairns2") (US Patent No: 6,268,841 B1) and Nitta et al. (US Patent No: 6,661,402 B1).

As for claim 3, Cairns1teaches that the digital-analog converter part (Fig. 4, item 12, section [0019]) and a demultiplexer part (Fig. 4, item 14, section [0016]).

Cairns1 fails to teach of a second multiplexer part.

Cairns2 teaches of a second multiplexer part (Fig. 11b, items 47, 49, column 10, lines 9-12).

It would have been obvious to one with ordinary skill in the art at the time the invention was made to include the second multiplexer of Cairns2 with the DAC of Cairns1 in order to provide the apparatus with a data line driver where there are more data lines than data line circuits (Cairns2, column 4, lines 21-25).

Cairns1 and Cairns2 fails to teach of a positive digital-analog converter converting the digital pixel data to a positive pixel signal; a negative digital-analog converter converting the digital pixel data to a negative pixel signal in accordance with a polarity control signal.

Nitta teaches of a positive digital-analog converter (Fig. 2, item 228, column 3, lines 24-26) converting the digital pixel data to a positive pixel signal; a negative digital-analog converter (Fig. 2, item 229, column 3, lines 27-31) converting the digital pixel data to a negative pixel signal in accordance with a polarity control signal (Fig. 2, item 425, column 6, lines 50-53).

It would have been obvious to one with ordinary skill in the art at the time the invention was made to combine separate the signals in accordance to their polarity as taught by Nitta with the driving circuitry of Cairns1 and Cairns2 in order to improve the picture quality by providing a more efficient driving method (Nitta, column 1, lines 50-55).

As for claim 32, Cairns1 and Cairns2 fails to teach of time-divided digital pixel data comprises: converting the time-divided pixel data to a positive analog pixel signal and a negative analog pixel signal; and selecting one of the positive and the negative analog pixel signals in accordance with a polarity control signal.

Nitta teaches that the time-divided digital pixel data comprises: converting the time-divided pixel data to a positive analog pixel signal and a negative analog pixel signal; and selecting one of the positive and the negative analog pixel signals in accordance with a polarity control signal (column 3, lines 23-33; column 4, lines 35-30 and Fig. 2).

It would have been obvious to one with ordinary skill in the art at the time the invention was made to combine separate the signals in accordance to their polarity as taught by Nitta with

the driving circuitry of Cairns1 and Cairns2 in order to improve the picture quality by providing a more efficient driving method (Nitta, column 1, lines 50-55).

5. Claims 2, 14-29, 35-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cairns et al. ("Cairns1") (US Patent Application: 2002/0030652 A1), in view of Cairnes et al. ("Cairns2") (US Patent No: 6,268,841 B1), Enami et al (US Patent No: 5,892,493), and Nitta et al. (US Patent No: 6,661,402 B1).

As for independent claim 9, most of the claim limitations are rejected in claims 1, 30 above.

Cairns1 and Cairns2 fails to teach of the components of the driving apparatus having selected polarity.

Nitta teaches of the components of the driving apparatus having selected polarity via positive and negative output channels/paths in column 3, lines 23-33 and in column 4, lines 25-30.

It would have been obvious to one with ordinary skill in the art at the time the invention was made to have selected polarity as taught by Nitta with the various components of the driving apparatus of taught by Cairn1 in order to increase the speed and functionality of the driver (see Nitta: column 1, lines 50-55).

As for independent claim 35, see the rejection of claims 1, 9, 30 above.

As for claim 10, Cairns1 as modified by Cairns2, Enami and Nitta teaches that the digital-analog converter (Cairns1, Fig. 4, item 12) part comprises: a positive digital-analog converter (Cairns1, Fig. 4, item 12) converting the pixel signals provided through positive output channels of the multiplexer into positive pixel signals; and a negative digital-analog converter (Cairns1, Fig. 4, item 12) converting the pixel signals provided through negative output channels of the multiplexer into negative pixel signals (Cairns1, section [0015]) (Nitta, column 3, lines 23-33; column 4, lines 35-30).

As for claim 11, Cairns1 as modified by Cairns2, Enami and Nitta teaches that the multiplexer part (Cairns1, Fig. 4, item 13) comprises: a plurality of positive path switches coupled to input channels for the pixel data and commonly connected to positive output channels; and a plurality of negative path switches coupled to the input channels for the pixel data in parallel, connected to the positive path switches in parallel, and commonly connected to negative output channel (Cairns1, Fig.4, section [0015]) (Nitta, Fig. 2, column 3, lines 23-33; column 4, lines 35-30).

As for claim 12, Cairns1 as modified by Cairns2, Enami and Nitta teaches that the demultiplexer (Cairns1, Fig. 4, item 14) part comprises: a plurality of positive path switches forming a plurality of different positive paths, and commonly connected to a positive digital-analog converter, wherein the positive path switches connected to output channels of the positive digital-analog converter (Id.); and a plurality of negative path switches forming a plurality of different negative paths, commonly connected to a negative digital-analog converter (Id.),

wherein the negative path switches are connected to the positive path switches in parallel and connected to the positive channel switches of the output channels of the negative digital-analog converter (Cairns1, Fig.4, section [0015]) (Nitta, Fig. 1, column 3, lines 23-33; column 4, lines 35-30).

As for claim 14, Cairns1 as modified by Cairns2, Enami and Nitta teaches that the sampling part (Cairns2, Fig. 11b) and the holding part sample and hold the pixel signals supplied for the second period through the channel different from that of the pixel signal supplied for the first period (Cairns2, Fig. 12, each column has at least three sets of buffers).

As for claim 15, Cairns1 as modified by Cairns2, Enami and Nitta teaches that the sampling part (Cairns2, Fig. 11b) has a second demultiplexer (Cairns2, Fig. 3, item 25) part comprising; a plurality of the positive path switches forming a plurality of different positive paths and connected to the output channels of the demultiplexer part (Id.); and a plurality of negative path switches connected to the output channels of the demultiplexer (Id.), and connected to the positive path switches in parallel (Cairns2, Fig. 12, column 10, lines 18-41) (Nitta, Fig. 2, column 3, lines 23-33; column 4, lines 35-30).

As for claim 16, Cairns1 as modified by Cairns2, Enami and Nitta teaches that the holding part comprises: a positive path capacitor charging and holding the positive pixel signals from the positive path switches of the second demultiplexer (Cairns2, Fig. 3, item 25) part; and a negative path capacitor charging and holding the negative pixel signals from the negative path

switches of the second demultiplexer (Id.) part in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 17, Cairns1 as modified by Cairns2, Enami and Nitta teaches that the discharging part comprises: a plurality of positive path switches connected to the positive path switches of the second demultiplexer (Cairns1, Fig. 4, item 14) through the holding part and connected to the data lines; and a second demultiplexer (Id.) part having the negative path switches connected to the negative switches of the second demultiplexer (Id.) through the holding part and connected to the negative channel switches and the data lines in parallel in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 18, Cairns1 as modified by Cairns2, Enami and Nitta teaches that the multiplexer, the demultiplexer (Cairns2, Fig. 3, item 25), and the second demultiplexer (Id.) are controlled by a first control signal through an input polarity control signal and an ODD/EVEN signal performing the time-division on a horizontal period in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 19, Cairns1 as modified by Cairns2, Enami and Nitta teaches that the ODD/EVEN signal performsthe time-division on an enable period determined by a source output enable signal for the horizontal period in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 20, Cairns1 as modified by Cairns2, Enami and Nitta teaches that the ODD/EVEN signal further performs the time-division on a disable period of the source output enable signal in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 21, Cairns1 as modified by Cairns2, Enami and Nitta teaches that the multiplexer part, the demultiplexer (14) part in Fig.4 and section [0015] {Cairns1} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}. The combination of Cairns2 and Nitta teaches that the second demultiplexer (64) part recharge the holding part with the pixel signals for the disable period, wherein the pixel signals are generated for a previous enable period in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 22, Cairns1 as modified by Cairns2, Enami and Nitta teaches that the source output enable signal is generated by increasing the disable period of an external reference source output enable signal in order to secure a recharging period of the holding part in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 23, Cairns1 as modified by Cairns2, Enami and Nitta teaches the second multiplexer part is controlled by the first control signal and a second control signal that is phase-

inversed with respect to the first control signal in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 24, Cairns1 as modified by Cairns2, Enami and Nitta teaches that an output buffer (Cairns2, Fig. 11b, item 40) part buffering the pixel signal discharged from the holding part to the discharging part in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 25, Cairns1 as modified by Cairns2, Enami and Nitta teaches that the output buffer (Cairns2, Fig. 11b, item 40) part comprises: a plurality of positive path output buffers (Id.) connected between the positive path capacitors of the holding part and the positive path switches of the second multiplexer part; and a plurality of negative path output buffers (Id.) connected between the negative path capacitors of the holding part and the negative path switches of the second multiplexer part in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 26, Cairns1 as modified by Cairns2, Enami and Nitta teaches that the output buffer (Cairns2, Fig. 11b, item 40) part buffering the pixel signal supplied through the output channels of the second multiplexer part and supplying the pixel signals to each of the data lines in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 27, Cairns1 as modified by Cairns2, Enami and Nitta teaches that the output buffer (Cairns2, Fig. 11b, item 40) part comprises: a plurality of output buffers (Cairns2, Fig. 11b, item 40) connected between the output channels of the second multiplexer part and the data lines in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 28, Cairns1 as modified by Cairns2, Enami and Nitta teaches of: a shift register (Cairns1, Fig. 4, item 10) sequentially shifting an input source start pulse in accordance with an input source shift clock to generate a sampling signal; a latch part (Cairns1, Fig. 4, item 11) latching pixel data and simultaneously providing the multiplexer part with the latched pixel data for the enable period of the input source output enable signal; and a level shifter part raising a voltage of the pixel data from the multiplexer part to supply the pixel data to the digital-analog convert part in Fig.4 and section [0015] {Cairns1} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 29, Cairns1 as modified by Cairns2, Enami and Nitta teaches of: teaches that a third multiplexer part supplying the pixel signals from the output part to the corresponding data lines for the enable period of the source output enable signal and commonly supplying a reference voltage of the liquid crystal cells to the corresponding data lines for the disable period of the source output enable signal in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 36, Cairns1 as modified by Cairns2, Enami and Nitta teaches of: teaches that the performing a time-division on a digital pixel data and the converting the time-divided digital pixel data are controlled by an input polarity control signal and a first control signal through an ODD/EVEN signal performing a time-division on a horizontal period in Fig. 4 and in section [0015] {Cairns1} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 37, Cairns1 as modified by Cairns2, Enami and Nitta teaches of: teaches that the ODD/EVEN signal performs a time-division on an enable period determined by a source output enable signal in Fig. 4 and in section [0015] {Cairns1} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 38, Cairns1 as modified by Cairns2, Enami and Nitta teaches of: teaches that the ODD/EVEN signal performs a time-division on a disable signal of a source output enable signal in Fig. 4 and in section [0015] {Cairns1} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 39, Cairns1 as modified by Cairns2, Enami and Nitta teaches of: teaches the pixel signals are sampled and held by the ODD/EVEN signal for the disable period, wherein the pixel signals in a present enable period are the same as the pixel signals in a previous enable period in Fig. 4 and in section [0015] {Cairns1} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 40, Cairns1 as modified by Cairns2, Enami and Nitta teaches the disable period of the source output enable signal is determined by increasing the disable period of a reference source output enable signal inputted from an external source in Fig. 4 and in section [0015] {Cairns1} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 41, Cairns1 as modified by Cairns2, Enami and Nitta teaches that the outputting the held pixel signals is controlled by a first control signal and a second control signal having a phase inversion with respect to the first signal in Fig. 4 and in section [0015] {Cairns1} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 42, Cairns1 as modified by Cairns2, Enami and Nitta teaches the performing a time-division on a digital pixel data is carried out by outputting the time-divided pixel data with a polarity through the time-divided pixel data of the output channel opposite to that of the time-divided pixel data for a previous period and an adjacent channel in Fig. 4 and in section [0015] {Cairns1} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 43, Cairns1 as modified by Cairns2, Enami and Nitta teaches that the performing a time-division on a digital pixel data is carried out by converting the time-divided pixel data into the time-divided pixel data with a polarity opposite to that of the time-divided analog signal of a previous period and an adjacent channel in Fig. 4 and in section [0015] {Cairns1} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 44, Cairns1 as modified by Cairns2, Enami and Nitta teaches that the sampling and holding the time-divided analog pixel signals is performed by sampling and holding the time-divided pixel signal through a path with a polarity opposite to that of time-divided pixel signal of a previous period and an adjacent channel in Fig. 12 and in column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 45, Cairns1 as modified by Cairns2, Enami and Nitta teaches the output held pixel signals is buffered through an output buffer (Cairns2, Fig. 11b, item 40) part prior to supplying to the corresponding data lines, wherein the output buffer (Id.) part is connected to the corresponding data lines in Fig. 12 and in column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 46, Cairns1 as modified by Cairns2, Enami and Nitta teaches that the held pixel signals are supplied to the corresponding data lines for the enable period of an input source output enable signal, and a reference voltage of the liquid crystal cells is commonly supplied to the corresponding data lines for the disable period in Fig. 4 and in section [0015] {Cairns1} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 47, Cairns1 as modified by Cairns2, Enami and Nitta teaches of raising a voltage of the time-divided pixel data after the performing a time-division on a digital pixel data in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

Response to Arguments

6. Applicant's arguments filed 29 November 2006 have been fully considered but they are not persuasive.

7. In regards to the traversal of the Official Notice taken that for claim 1, it is well known in the art to include a third multiplexer, please see the additional teachings of Enami as shown above (Arg. 12).

8. In regards to the allegation that neither of the references teach of the amended claim language of having a "the sampling and holding first inputted pixel signals through a first part of the output channels and holding second inputted pixel signals from a second part of the output channels during a *first horizontal period*, and simultaneously supplying the first and second held pixel signals corresponding data lines during a *second horizontal period* (Arg. 12-14);" please refer to the table of Cairns2, Fig. 3.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tammy Pham whose telephone number is (571) 272-7773. The examiner can normally be reached on 8:00-5:30 (Mon-Fri).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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TP
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